In the Claims:

1. (Withdrawn) A method for minimizing the number of appearances of a given state in a code word generated from a data word comprising:

counting the number of times the given state appears in the data word;

if the count is greater than half of a total number of bits in the data word, then

inverting the data word;

setting a weight bit to the given state; and

else

setting the weight bit to an inverse of the given state.

2. (Withdrawn) The method of claim 1, wherein the code word comprises the weight bit combined with the inverted data word if the count is greater than half the total number of bits in the data word, else the code word comprises the weight bit combined with the data word.

3. (Withdrawn) The method of claim 2, wherein the weight bit is a single bit in length.

4. (Withdrawn) The method of claim 1, wherein the given state is a zero state, and the weight bit is set to zero if the number of zeros in the data word is greater than half the total number of bits in the data word, else the weight bit is set to one.

5. (Withdrawn) The method of claim 1, wherein the given state is a one state, and the weight bit is set to one if the number of ones in the data word is greater than half the total number of bits in the data word, else the weight bit is set to zero.

6. (Withdrawn) The method of claim 1, wherein the method can be used to generate code words for use in a transmission system with an asymmetrically terminated transmission line, and wherein the given state is complementary to the termination of the transmission line.

7. (Original) A circuit comprising:

an encoder coupled to a data input, the encoder containing circuitry to convert data words from the data input into code words with a minimized number of occurrences of a given state; and

a transmitter coupled to the encoder, the transmitter containing circuitry to inject the code words onto a transmission line, wherein the transmission line is asymmetrically terminated.

8. (Original) The circuit of claim 7, wherein the code word is one bit longer than the data word.

9. (Original) The circuit of claim 7, wherein the encoder comprises:

a weight calculator coupled to the data input, the weight calculator containing circuitry to determine a count of the number of times the given state appears in a data word and to compute a weight bit based on the count; and

a plurality of logic blocks coupled to the data input and the weight calculator, wherein each logic block is coupled to a single bit of the data input and the weight bit computed by the weight calculator, the logic block to combine the inputs to produce a bit of the code word.

10. (Original) The circuit of claim 9, wherein the logic block is implemented as an exclusive-nor (XNOR) logic gate.

11. (Original) The circuit of claim 9, wherein there is one logic block for each bit in the data word.

12. (Original) The circuit of claim 9, wherein the weight calculator comprises:

a first hierarchy of M switches, wherein M is less than the number of bits in the data word, wherein each switch is controlled by a bit of the data word, a switch to route an input to an output depending on the value of the bit controlling it;

a second hierarchy of switches, wherein for each switch in the first hierarchy of switches, there is a pair of switches in the second hierarchy of switches, wherein each pair of switches is controlled by a bit of the data word; and

a logic block coupled to the second hierarchy of switches, the logic block containing circuitry to compute the weight bit.

13. (Original) The circuit of claim 12, wherein one half of the data bits in the data word is coupled to the switches in the first hierarchy of switches and the remaining data bits in the data word are coupled to the pairs of switches in the second hierarchy of switches.

14. (Original) The circuit of claim 13, wherein if a data bit is used to control a switch in the first hierarchy of switches, then the data bit is not used to control a pair of switches in the second hierarchy of switches.

15. (Original) The circuit of claim 12, wherein an input to the switches in the first hierarchy of switches is a low voltage potential.

16. (Original) The circuit of claim 12, wherein each switch is a one input to two output switch, and wherein the inputs to a pair of switches in the second hierarchy of switches are the two outputs of a switch from the first hierarchy of switches.

17. (Original) The circuit of claim 12, wherein a switch can be implemented as a one-input to two-output multiplexer.

18. (Original) The circuit of claim 7, wherein the transmission line is pulled to a voltage potential.

19. (Original) The circuit of claim 18, wherein the transmission line is pulled to a high voltage potential and the given state is a low voltage potential.

20. (Original) The circuit of claim 18, wherein the transmission line is pulled to a low voltage potential and the given state is a high voltage potential.

21. (Original) A transmission system comprising:

an encoder coupled to a data input, the encoder containing circuitry to convert data words from the data input into code words with a minimized number of occurrences of a given state;

a transmitter coupled to the encoder, the transmitter containing circuitry to inject the code words onto a transmission line, wherein the transmission line is asymmetrically terminated;

a receiver coupled to the transmission line, the receiver containing circuitry to receive code words from the transmission line; and

a decoder coupled to the receiver, the decoder containing circuitry to convert code words into data words.

22. (Original) The transmission system of claim 21, wherein each code word comprises a code block and a weight bit, and wherein the decoder comprises a plurality of logic blocks coupled to the receiver, wherein each logic block is coupled to a single bit of the code block and the weight bit, the logic block to combine the inputs to produce a bit of the data word.

23. (Original) The transmission system of claim 22, wherein the logic block can be implemented as an exclusive-nor (XNOR) logic gate.